A Triple Redundant Latch Design with Low Delay Time

FIELD OF THE INVENTION

[001] This invention relates generally to latch design. More particularly, this invention relates to improving soft error immunity in latches.

BACKGROUND OF THE INVENTION

[002] High-energy neutrons lose energy in materials mainly through collisions with silicon nuclei that lead to a chain of secondary reactions. These reactions deposit a dense track of electron-hole pairs as they pass through a p-n junction. Some of the deposited charge will recombine, and some will be collected at the junction contacts. When a particle strikes a sensitive region of a latch, the charge that accumulates could exceed the minimum charge that is needed to "flip" the value stored on the latch, resulting in a soft error.

[003] The smallest charge that results in a soft error is called the critical charge of the latch. The rate at which soft errors occur (SER) is typically expressed in terms of failures in time (FIT).

[004] A common source of soft errors are alpha particles which may be emitted by trace amounts of radioactive isotopes present in packing materials of integrated circuits. "Bump" material used in flip-chip packaging techniques has also been identified as a possible source of alpha particles.

[005] Other sources of soft errors include high-energy cosmic rays and solar particles. High-energy cosmic rays and solar particles react with the upper atmosphere generating high-energy protons and neutrons that shower to the earth. Neutrons can be particularly troublesome as they can penetrate most man-made

construction (a neutron can easily pass through five feet of concrete). This effect varies with both latitude and altitude. In London, the effect is two times worse than on the equator. In Denver, Colorado with its mile-high altitude, the effect is three times worse than at sea-level San Francisco. In a commercial airplane, the effect can be 100-800 times worse than at sea-level.

[006] Radiation induced soft errors are becoming one of the main contributors to failure rates in microprocessors and other complex ICs (integrated circuits). Several approaches have been suggested to reduce this type of failure. Adding ECC (Error Correction Code) or parity in data paths approaches this problem from an architectural level. Adding ECC or parity in data paths can be complex and costly.

[007] At the circuit level, SER may be reduced by increasing the ratio of capacitance created by oxides to the capacitance created by p/n junctions. The capacitance in a latch, among other types, includes capacitance created by p/n junctions and capacitance created by oxides. Since electron/holes pairs are created as high-energy neutrons pass through a p/n junction, a reduction in the area of p/n junctions in a latch typically decreases the SER. Significant numbers of electron/hole pairs are not created when high-energy neutrons pass through oxides. As a result, the SER may typically be reduced by increasing the ratio of oxide capacitance to p/n junction capacitance in a SRAM cell.

[008] There is a need in the art to reduce the SER in latches. An embodiment of this invention reduces the SER in latches while adding only a small increase in physical size of the latch and a small increase in the delay time through the latch.

SUMMARY OF THE INVENTION

[009] In a preferred embodiment, the invention provides a circuit and method for a smaller and faster triple redundant latch. Three settable memory elements set an identical logical value into each settable memory element. After the settable memory elements are set, a voting structure with inputs from the first settable memory element, the second memory element, and control to the settable memory elements determines the logical value held on the third settable memory element. The propagation delay through the third settable memory element is the only propagation delay of the triple redundant latch.

[010] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[011] Figure 1 is a schematic of a triple redundant latch. Prior Art

[012] Figure 2 is a block diagram of an embodiment of an improved triple redundant latch.

[013] Figure 3 is a block diagram of an improved triple redundant latch.

[014] Figure 4 is a schematic of an improved triple redundant latch.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[015] Figure 1 is a schematic of a triple redundant latch. The input, **100,** to the triple redundant latch is connected to the input of transfer gates, **TG1**, **TG2**, and **TG3**. Control signal, **102**, is connected to transfer gates, **TG1**, **TG2**, and **TG3**. Control signal, **102**, controls when the signal on the input of transfer gates, **TG1**, **TG2**, and **TG3** is transferred to the outputs, **104**, **106**, and **108** of transfer gates, **TG1**, **TG2**, and **TG3** respectively. The signal presented to outputs, **104**, **106**, and **108**, is stored in **LATCH1**, **LATCH2**, and **LATCH3** respectively.

[016] After control signal, **102**, is turned off, the signal on **LATCH1** drives the input of inverter, **INV1**. After control signal, **102**, is turned off, the signal on **LATCH2** drives the input of inverter, **INV2**. After control signal, **102**, is turned off, the signal on **LATCH3** drives the input of inverter, **INV3**. The output, **110**, of inverter, **INV1**, drives an input to **AND1** and an input to **AND2**. The output, **112**, of inverter, **INV2**, drives an input to **AND1** and an input to **AND3**. The output, **114**, of inverter, **INV3**, drives an input to **AND2** and an input to **AND3**. The output, **116**, of **AND1** drives an input of **OR1**. The output, **118**, of **AND2** drives an input of **OR1**. The output, **120**, of **AND3** drives an input of **OR1**. The output of the triple redundant latch is the output, **122** of **OR1**.

[017] A triple redundant latch reduces soft errors by storing the same data in three different latches. For example, when the control signal, **102** is on, a logical high value may be driven from the inputs, **100**, of transfer gates, **TG1**, **TG2**, and **TG3** to the outputs, **104**, **106**, and **108**, of transfer gates, **TG1**, **TG2**, and **TG3** respectively.

After turning control signal **102** off, a logical high value is stored in latches, **LATCH1**, **LATCH2**, and **LATCH3**. The stored logical high value on **LATCH1** drives the input of inverter, **INV1**, and produces a logical low value on the output, **110**, of inverter, **INV1**. The stored logical high value on **LATCH2** drives the input of inverter, **INV2**, and produces a logical low value on the output, **112**, of inverter, **INV2**. The stored logical high value on **LATCH3** drives the input of inverter, **INV3**, and produces a logical low value on the output, **114**, of inverter, **INV3**.

[018] Since the output, **110**, **112**, and **114** of inverters, **INV1**, **INV2**, and **INV3**, respectively, are low, all the inputs, **110**, **112**, and **114** to **AND1**, **AND2**, and **AND3** respectively are a logical low value. Since all the inputs, **110**, **112**, and **114**, to **AND1**, **AND2**, and **AND3** respectively are a logical low value, the output, **116**, **118**, and **120** of **AND1**, **AND2**, and **AND3** respectively are a logical low value. Since the output, **116**, **118**, and **120** of **AND1**, **AND2**, and **AND3,** respectively are a logical low value, all the inputs of **OR1** are a logical low value. Since all the inputs, **116**, **118**, and **120** to **OR1** are logical low value, the output, **122**, is logical low value.

[019] If a soft error occurs, for example, in **LATCH2**, and changes the stored logical value from a logical high value to a logical low value, a logical low value is now presented to the input, **106**, of inverter, **INV2**. The output, **112**, of inverter, **INV2**, presents a logical high value to an input of **AND1** and **AND3**. Since, in this example, the other input, **110** to **AND1** and the other input, **114**, to **AND3**, is a logical low value, the output, **116** and **120** of **AND1** and **AND3** respectively remains a logical low value and the output, **122**, does not change. This example illustrates how a single soft error in one latch does not change the original stored value in a triple redundant latch.

[020] As a further example, assume, in addition to the soft error in **LATCH2**, there is an additional soft error in **LATCH3**. Now, the input, **108**, to inverter, **INV3**, is a logical low value and as a result, the output, **114**, of inverter, **INV3**, is a logical high value. A logical high value in now presented to an input, **114**, of **AND2**, and to an input, **114**, of **AND3**. Since a logical low and logical high value are presented on the inputs of **AND1**, the output, **116** of **AND1** is still a logical low value. Since a logical low and logical high value are presented on the inputs of **AND2**, the output, **118** of **AND2** is still a logical low value. However, since inputs, **112** and **114**, to **AND3** are a logical high value, the output, **120**, is a logical high value. Since input, **120**, to **OR1** is a logical high value, the output, **122**, changes from a logical low value to a logical high value. This example illustrates how soft errors in two latches of a triple redundant latch do change the original stored value of the triple redundant latch.

[021] A triple redundant latch prevents a single soft error from changing the original value stored in the latch. However, this comes at the cost of additional circuitry which results in a physically larger latch. In addition, a triple redundant may introduce time delay in the delay path of the latch. As consequence, a triple redundant latch is usually larger and slower than a single latch.

[022] Figure 2 is a block diagram of an embodiment of an improved triple redundant latch. In this embodiment, an identical logical value, **210**, is set into settable memory element1, **SME1**, settable memory element2, **SME2**, and settable memory element3, **SME3**, by controlling signal **204**. After an identical logical value, **210**, is set into settable memory element1, **SME1**, settable memory element2, **SME2**, and settable memory element3, **SME3**, by controlling signal **204**, the identical logical value is held in all three settable memory elements, **SME1**, **SME2**, and **SME3**. The voting structure, **VS**, after an identical logical value, **210**, is set into settable memory

element1, **SME1**, settable memory element2, **SME2**, and settable memory element3, **SME3**, determines the logical value, **218**, stored in settable memory element three, **SME3**, based on the logical values presented to input, **214**, input, **216**, and control signal, **204**.

[023] If the logical value, **218**, stored in settable memory element three, **SME3**, is disturbed by a soft error event, the voting structure, **VS**, will restore the original logical value stored in settable memory element three, **SME3**. If the logical value stored in settable memory element one, **SME1**, is disturbed by a soft error event, the voting structure, **VS**, will tri-state its output, **218**, leaving the original logical value stored in settable memory element three, **SME3**. If the logical value stored in settable memory element two, **SME2**, is disturbed by a soft error event, the voting structure, **VS**, will tri-state its output, **218**, leaving the original logical value stored in settable memory element three, **SME3**. If any two settable memory elements are disturbed by a soft error event, the logical value original stored in the triple redundant latch may fail.

[024] The delay time through the triple redundant latch shown in Figure 2 is determined by a small amount of capacitance added by the voting structure, **VS**, and the propagation delay of the settable memory element3, **SME3**. This embodiment of the invention significantly improves the delay time of a triple redundant latch. The delay time through the prior art shown in Figure 1, for example, includes the propagation delay through the slowest latch among latches **LATCH1**, **LATCH2**, and **LATCH3**, the propagation delay through an inverter, **INV2**, the propagation delay through an AND gate, **AND2**, and the propagation delay through an OR gate, **OR1**.

[025] Figure 3 is a block diagram of a triple redundant latch with improved delay and size. The input of the triple redundant latch shown in this example is

connected to the inputs, **302**, of transfer gates, **TG1**, **TG2**, and **TG3**. In addition, a tristatable input inverter, a cross-coupled NAND gate, and a cross-coupled NOR gate may used in place of a transfer gate. If the control signals, **304** and **306**, are on, the signal at the input, **302**, of transfer gates, **TG1**, **TG2**, and **TG3**, is transferred to the output, **308**, of transfer gate, **TG1**, the output, **310**, of transfer gate, **TG2**, and the output, **312** of transfer gate, **TG3**. The logical value presented on the output, **308**, of transfer gate **TG1**, is also an input to latch1, **L1**. The logical value presented on the output, **312**, of transfer gate **TG3**, is also an input to latch2, **L2**. The logical value presented on the output, **310**, of transfer gate **TG2**, is also connected to the output, **310**, of the majority voter, **MAJVT**, and the input/output, **310**, of latch3, **L3**.

[026] The output, **314**, of latch1, **L1**, is connected to an input, **314**, of the majority voter, **MAJVT**. The output, **316**, of latch2, **L2**, is connected to an input, **316**, of the majority voter, **MAJVT**. Control signals, **304**, and **306**, are also connected to inputs of the majority voter, **MAJVT**.

[027] As an example of how redundancy applies for this embodiment, assume that a logical high value is stored. Storage nodes **308**, **310**, and **312** each have a logical high value stored in this example. The output, **314**, of latch1, **L1**, provides a logical low value to an input of the majority voter, **MAJVT**. The output, **316**, of latch1, **L2**, provides a logical low value to an input of the majority voter, **MAJVT**. The control signals, **304** and **306**, provide a logical low value and a logical high value respectively to two inputs of the majority voter, **MAJVT**. As a result of the logical values presented to the majority voter, **MAJVT**, the output, **310**, of the majority voter, **MAJVT**, is driven high to match the logical high value stored on latch3, **L3**.

[028] If, in this example, a soft error event changes the logical value stored on latch1, **L1**, from a logical high value to a logical low value, the logical value stored on

latch3, **L3**, will retain its logical high value because the output, **310**, of the majority voter, **MAJVT**, is tri-stated. As a result, the triple redundant latch retains the original logical value stored on it despite a single soft error.

[029] If in this example a soft error event changes the logical value stored on latch1, **L2**, from a logical high value to a logical low, the logical value stored on latch3, **L3**, will retain its logical high value because the output, **310**, of the majority voter, **MAJVT**, is tri-stated. As a result, the triple redundant latch retains the original logical value stored on it despite a single soft error.

[030] If in this example a soft error event changes the logical value stored on latch1, **L3**, from a logical high value to a logical low, the majority voter, **MAJVT**, will drive input/out, **310**, of latch3, **L3**, back to a logical high value. As a result, the triple redundant latch retains the original logical value stored on it despite a single soft error.

[031] If, however, in this example, a soft error event changes the values stored on nodes **308** and **312**, the triple redundant latch will change from its original value. If a soft error event changes the logical values stored on nodes **308** and **312**, from logical high values to a logical low values, the inputs, **314** and **316**, to the majority voter, **MAJVT**, change from logical low values to logical high values. As a result of having logical high values on the inputs, **314** and **316**, the majority vote is a logical low value. As a result, the logical value stored on node **310** is changed from the original logical high value to a logical low value. In this example, the original value stored in the triple redundant latch is changed from a logical high value to a logical low value.

[032] In addition to improving the soft error rate of a latch, the triple redundant latch shown in Figure 3, also reduces the physical size of a triple redundant

latch because it uses fewer transistors. The triple redundant latch shown in Figure 3 also reduces the delay time through a triple redundant latch because the number of logic delays is reduced.

[033] Figure 4 is a schematic of an improved triple redundant latch. Figure 4 contains the same basic blocks that Figure 3 contains; transfer gate 1, **TG1**, transfer gate 2, **TG2**, transfer gate 3, **TG3**, latch1, **L1**, latch2, **L2**, latch3, **L3**, and majority voter, **MAJVT**.

[034] An embodiment of a transfer gate 1, **TG1**, for the triple redundant latch contains a PFET, **MP2** and an NFET **MN2**. In this embodiment, the drains of PFET, **MP2**, and NFET, **MN2**, are connected to the input, **402**, of transfer gate 1, **TG1**. The sources of PFET, **MP2**, and NFET, **MN2**, are connected to the output, **408**, of transfer gate 1, **TG1**. The gate of PFET, **MP2**, is connected to the control input, **406**, of transfer gate 1, **TG1**. The gate of NFET, **MN2**, is connected to the control input, **404**, of transfer gate 1, **TG1**.

[035] An embodiment of a transfer gate 2, **TG2**, for the triple redundant latch contains a PFET, **MP3** and an NFET **MN3**. In this embodiment, the drains of PFET, **MP3**, and NFET, **MN3**, are connected to the input, **402**, of transfer gate 2, **TG2**. The sources of PFET, **MP3**, and NFET, **MN3**, are connected to the output, **416**, of transfer gate 2, **TG2**. The gate of PFET, **MP3**, is connected to the control input, **406**, of transfer gate 2, **TG2**. The gate of NFET, **MN3**, is connected to the control input, **404**, of transfer gate 2, **TG2**.

[036] An embodiment of a transfer gate 3, **TG3**, for the triple redundant latch contains a PFET, **MP4** and an NFET **MN4**. In this embodiment, the drains of PFET, **MP4**, and NFET, **MN4**, are connected to the input, **402**, of transfer gate 3, **TG3**. The sources of PFET, **MP4**, and NFET, **MN4**, are connected to the output, **412**, of transfer

gate 3, **TG3**. The gate of PFET, **MP4**, is connected to the control input, **406**, of transfer gate 3, **TG3**. The gate of NFET, **MN4**, is connected to the control input, **404**, of transfer gate 3, **TG3**.

[037] An embodiment of latch1, **L1**, for the triple redundant latch contains PFET, **MP5**, NFET, **MN5**, PFET, **MP6**, and NFET, **MN6**. In this embodiment, the gate of PFET, **MP5**, and the gate of NFET, **MN5**, is connected to the drain of PFET, **MP6** and to the drain of NFET, **MN6**, the input, **408**, of latch1, **L1**. The drain of PFET, **MP5**, and the drain of NFET, **MN5**, is connected to the gate of PFET, **MP6** and to the gate of NFET, **MN6**, the output, **410**, of latch1, **L1**. The sources of PFET, **MP5** and PFET, **MP6** are connected to **VDD**. The sources of NFET, **MN5**, and NFET, **MN6** are connected to **GND**.

[038] An embodiment of latch2, **L2**, for the triple redundant latch contains PFET, **MP7**, NFET, **MN7**, PFET, **MP8**, and NFET, **MN8**. In this embodiment, the gate of PFET, **MP7**, and the gate of NFET, **MN7**, is connected to the drain of PFET, **MP8** and to the drain of NFET, **MN8**, the input, **412**, of latch2, **L2**. The drain of PFET, **MP7**, and the drain of NFET, **MN7**, is connected to the gate of PFET, **MP8** and to the gate of NFET, **MN8**, the output, **414**, of latch2, **L2**. The sources of PFET, **MP7** and PFET, **MP8** are connected to **VDD**. The sources of NFET, **MN7**, and NFET, **MN8** are connected to **GND**.

[039] An embodiment of latch3, **L3**, for the triple redundant latch contains PFET, **MP12**, NFET, **MN12**, PFET, **MP13**, and NFET, **MN13**. In this embodiment, the gate of PFET, **MP12**, and the gate of NFET, **MN12**, is connected to the drain of PFET, **MP13** and to the drain of NFET, **MN13**, the input/output, **416**, of latch3, **L3**. The drain of PFET, **MP12**, and the drain of NFET, **MN12**, is connected to the gate of PFET, **MP13** and to the gate of NFET, **MN13**, node **426**, of latch3, **L3**. The sources

of PFET, **MP12** and PFET, **MP13** are connected to **VDD**. The sources of NFET, **MN12**, and NFET, **MN13** are connected to **GND**.

[040] An embodiment of a majority voter, **MAJVT**, for the triple redundant latch contains PFET, **MP9**, PFET, **MP10**, PFET, **MP11**, NFET, **MN9**, NFET, **MN10**, and NFET, **MN11**. In this embodiment, the gates of PFET, **MP10**, and NFET, **MN10**, are connected to the first input, **410**, of the majority voter, **MAJVT**. The gates of PFET, **MN9**, and NFET, **MN11**, are connected to the second input, **414**, of the majority voter, **MAJVT**. The gate of PFET, **MP11**, is connected to the third input, **404**, of the majority voter, **MAJVT**. The gate of NFET, **MN9**, is connected to the fourth input, **406**, of the majority voter, **MAJVT**. The source of PFET, **MP9**, is connected to **VDD**. The source of NFET, **MN11**, is connected to **GND**. The drain, **418**, of PFET, **MP9**, is connected to the source of PFET, **MP10**, **418**. The drain, **420**, of PFET, **MP10**, is connected to the source of PFET, **MP11**, **420**. The drain of PFET, **MP11** and the drain of NFET, **MN9** are connected to the output, **416**, of the majority voter, **MAJVT**. The source, **422**, of NFET, **MP9**, is connected to the drain of NFET, **MN10**, **422**. The source, **424**, of NFET, **MN10**, is connected to the drain of NFET, **MN11**, **424**.

[041] Figure 4 is a schematic of an improved triple redundant latch. An input signal drives the inputs, **402**, of transfer gate 1, **TG1**, transfer gate 2, **TG2**, and transfer gate 3, **TG3**. If control signal, **404** is a logical high value and control signal, **406**, is a logical low value, the signal at the input, **402**, of transfer gate 1, **TG1**, transfer gate 2, **TG2**, and transfer gate 3, **TG3** is transferred to the output, **408**, of transfer gate 1, **TG1**, the output, **416**, of transfer gate 2, **TG2**, and the output, **412**, of transfer gate 3, **TG3**.

[042] The signal transferred to nodes **408**, **416**, and **412** is also presented to the input, **408**, of latch1, **L1**, the input, **412**, of latch2, **L2**, the input/output, **416**, of latch3, **L3**, and the output, **416** of the majority voter, **MAJVT**. Latches **L1**, **L2**, and **L3** store the same signal. The outputs, **410** and **414**, of latches, **L1** and **L2** respectively, output the opposite sense of the signal stored. The outputs, **410** and **414**, of latches, **L1** and L2 respectively, along with the first, **404**, and second, **406**, control signals are inputs to the majority voter, **MAJVT**. The inputs, **404**, **406**, **410**, and **414**, into the majority voter, **MAJVT**, cause the majority voter, **MAJVT**, to reinforce the signal presented at the output, **416**, of transfer gate 2, **TG2**.

[043] After control input, **404**, is driven to a logical low value, and control input, **406**, is driven to a logical high value, latch1, **L1**, latch2, **L2**, and latch3, **L3** store the original logical value presented on nodes **408**, **412**, and **416**, respectively. If none of the nodes, **408**, **412**, and **416**, is disturbed, then a signal of the same sense is presented on the output, **416**, of the majority voter, **MAJVT**.

[044] For example, if a logical high value is stored on nodes **408**, **412**, and **416**, then a logical high value is presented on the output, **416**, of the majority voter, **MAJVT**. A logical low value on the output, **410**, of latch1, **L1**, is applied to the first input of the majority voter, **MAJVT**. A logical low value on the output, **414**, of latch2, **L2**, is applied to the second input of the majority voter, **MAJVT**. Since in this example, the transfer gates are turned off, control signal **404**, is low and control signal **406**, is high. Because control signal **404** is low, a logical low value is applied to the third input of the majority voter, **MAJVT**. Because control signal **406** is high, a logical high value is applied to the fourth input of the majority voter, **MAJVT**. With these logical values applied to the majority voter, **MAJVT**, the output, **416**, of majority voter, **MAJVT**, remains a high logical value.

[045] If in this example where a logical high value is stored on nodes, **408**, **412**, and **416** , node **408** is changed to a logical low value by a soft error event, a logical high value is then presented to input, **410**, of the majority voter, **MAJVT** . Inputs, **414**, and **404**, remain a logical low value while input **406** remains a logical high value. Since input, **410**, has changed from a low logical value to a high logical value, node **416**, is no longer actively driven high by the majority voter, **MAJVT**. However, since latch3, **L3** has not been disturbed, latch3, **L3**, actively holds node **416** at a logical high value. As a consequence, despite latch1, **L1**, being disturbed by a soft error event to a logical low value, the value on the output, **428**, of the triple redundant latch remains a logical high value.

[046] If, however, a soft error event changes the value stored on node, **408** and node, **412**, the triple redundant latch will change from its original value. For example, if a logical high value is stored on nodes **408**, **412**, and **416**, a logical high value is presented on the output, **416**, of the majority voter, **MAJVT**. If a soft error event changes the logical value stored on nodes, **408** and **412**, from a logical high value to a logical low value, inputs, **410** and **414**, into the majority voter, **MAJVT**, change from logical low values to logical high values. Since inputs, **410** and **414**, of the majority voter, **MAJVT**, are a logical high value, and control signal, **406**, remains a logical high value, the majority voter output, **416**, is pulled to a logical low value. The high logical value stored on latch3, **L3**, is then flipped to a logical low value. The output, **428**, of the triple redundant latch, is then changed from a logical low value to a logical high value.

[047] If a single soft error event temporally changes the logical value stored in latch3, **L3**, the majority voter, **MAJVT**, will reset the logical value on latch3, **L3**, to its original value. The logical state on latch3, **L3**, is reset to its original value

because none of the inputs, **404**, **406**, **310**, and **414**, on the majority voter, MAJVT, has changed as a consequence of latch3, **L3**, changing its logical value. Therefore, the output, **416**, of the majority voter, **MAJVT**, drives latch3, **L3**, back to its original value.

[048] The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and other modifications and variations may be possible in light of the above teachings. The embodiment was chosen and described in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments of the invention except insofar as limited by the prior art.